40G-PSM4 QSFP+ Transceiver

QSP1PF4LxC000ExG

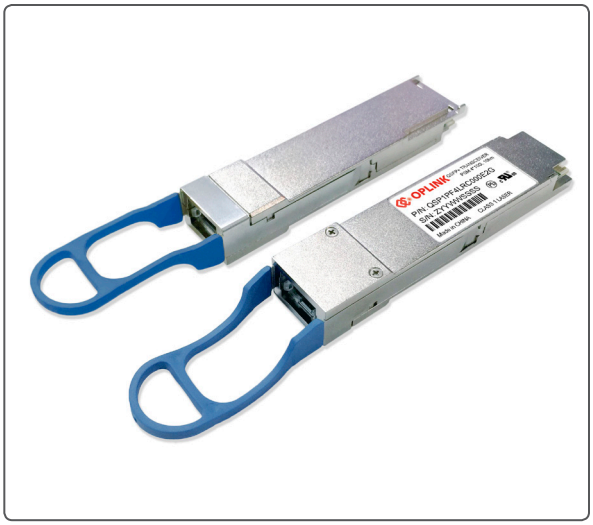
Product Description

The QSP1PF4LxC000ExG is a hot pluggable fiber optic transceiver in the QSFP+ form factor with digital diagnostics monitoring functionality (DDM) and control function. The QSFP+ PSM4 module has four identical and independent lanes which provides a point-to-point 40Gb/s link over eight single mode fibers up to 10km. This makes it an ideal low cost solution for long reach data center optical interconnects.

The central wavelength of each lane is at 1310nm wavelength. The low power consumption and excellent EMI performance enable system design with high port density. The product is designed and tested in accordance with industry safety standards. The transceiver is Class 1 Laser product per U.S. FDA/CDRH and IEC 60825-1:2007 & IEC 60825-2:2004+A1+A2standards.

The transceiver can be conveniently assembled into and released from the host system through the latch.

The transceiver operates from a single +3.3V power supply over an operating case temperature range of -5°C to +70°C. The housing is made of metal for EMI immunity.



Features

- ☑ Four lanes (per direction) with MPO optical interface
- ☑ Support OC192/STM-64, 10GBASE-LR, OTU2, OTU1e and OTU2e per lane in single mode fiber
- ☑ Transmission distance options of 10km & 2km
- ☑ QSFP+ MSA compliant
- ☑ Maximum 3.5W operation power
- ☑ RoHS 6/6 compliant
- ☑ Laser Class 1 IEC/CDRH compliant

Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
Storage Temperature Range		T_{ST}	- 40	+ 85	°C
Case Operating Temperature	Commercial	T_{OP}	- 5	+ 70	°C
Operating Relative Humidity [1]		RH	0	85	%
Supply Voltage Range		V_{CC}	- 0.5	+ 3.6	V
[1] *Non condensing*					

Transmitter Performance Characteristics (Over Operating Case Temperature. V_{CC} = 3.13 to 3.47V)

Parameter	Symbol	Single Rate			Multi Rate			Units
		Min	Typ	Max	Min	Typ	Max	
Data Rate (per Lane)	*B*	-	10.31	-	9.95	-	11.09	Gb/s
Lane Wavelength	λ_C	1260	-	1355	1260	-	1355	nm
Spectral width (DFB, for 10km)	$\Delta\lambda_{20}$	-	-	1.0	-	-	1.0	nm
Average Optical Output Power (per Lane) [1]	P_{AVG}	- 8.2	-	0.5	- 6.0	-	0.5	dBm
Launch power in OMA minus TDP	-	- 6.2			- 6.2	-	-	dBm
Optical Modulation Amplitude, for 10km (per Lane)	P_{OMA}	- 5.2	-	-	- 5.2	-	-	dBm
Extinction Ratio	*ER*	3.5	-	-	6.0	-	-	dB
Side Mode Suppression Ratio (DFB)	*SMSR*	30	-	-	30	-	-	dB
Optical Return Loss Tolerance	-	-	-	- 12	-	-	- 12	dB
Average Launch Power of OFF Transmitter		-	-	- 30	-	-	- 30	dBm
Transmitter and Dispersion Penalty@10.3G (per Lane)	*TDP*	-	-	3.2	-	-	3.2	dB
Optical Output Eye		*Compliant with IEEE 802.3ba {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}*			*5%@BOL*			

[1] Average power figures are informative only.

Receiver Performance Characteristics (Over Operating Case Temperature. V_{CC} = 3.13 to 3.47V)

Parameter		Symbol	Single Rate			Multi Rate			Units
			Min	Typ	Max	Min	Typ	Max	
Data Rate		*B*	-	10.31	-	9.95	-	11.09	Gb/s
Wavelength of Operation (per Lane)		λ_C	1260	-	1355	1260	-	1355	nm
Receiver Sensitivity (10km)	AOP @ 11.09Gb/s [1]	P_{min}	-	-	-	-	-	- 11.0	dBm
	P_{AVG} @ 10.3125Gb/s [1]		-	-	- 14.4	-	-	-	
	OMA @ 10.3125 Gb/s		-	-	- 12.6	-	-	-	
Receiver Sensitivity (2km)	P_{AVG} @ 10.3125Gb/s [1]	P_{min}	-	-	- 13.5	-	-	-	dBm
	OMA @ 10.3125 Gb/s		-	-	- 11.5	-	-	-	
Stressed receiver sensitivity in OMA [2] @9.95Gb/s and 10.3Gb/s		-	-	-	- 10.3	-	-	- 10.3	dBm
Maximum Input Power (10^{-12} BER)		P_{max}	+ 0.5	-	-	+ 0.5	-	-	dBm
Receiver Reflectance		-	-	-	- 12	-	-	- 14	dB
LOS Hysteresis		-	0.5	-	-	0.5	-	-	dB
LOS Thresholds	Increasing Light Input	P_{los+}	-	-	- 16	-	-	16	dBm
	Decreasing Light Input	P_{los-}	- 30	-	-	- 30	-	-	

[1] Specified with BER <1x10^{-12} and PRBS 2^{31}-1, informative
[2] The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits

Note: The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature. The Rx parameters are measured at TP3 point defined in IEEE 802.3ba.

Transmitter Electrical Characteristics (Over Operating Case Temperature. V_{CC} = 3.13 to 3.47V)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Differential Input Impedance	Z_d	-	100	-	Ω
Differential Input Voltage Swing	$V_{PP-DIFF}$	-	-	800	mV

Receiver Electrical Interface (Over Operating Case Temperature. V_{CC} = 3.13 to 3.47V)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Differential Output Impedance	Z_d	-	100	-	Ω
Differential Output Swing	$V_{PP-DIFF}$	250	-	1600	mV
Output Rise and Fall time (20% to 80%)	t_{RH}, t_{FH}	28	-	-	ps

Electrical Power Supply Characteristics (Over Operating Case Temperature. V_{CC} = 3.13 to 3.47V)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Power Supply Voltage		V_{CC1} V_{CCTx} V_{CCRx}	3.13	3.30	3.47	V
Supply Current		I_{VCC}	-	-	1	A
Power Consumption		P_W	-	-	3.5	W
Power Consumption	LP mode	-	-	-	1.5	W

Note: The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature.

Laser Safety:
All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825 standards. They must be operated under specified operating conditions.

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This product complies with
21 CFR 1040.10 and 1040.11
Meets Class 1 Laser Safety Requirements

Electrical Pin Definition

Pin	Symbol	Description	Plug Sequence	Pin	Symbol	Description	Plug Sequence
1	GND	Ground [1]	1	20	GND	Ground [1]	1
2	Tx2n	Transmitter Inverted Data Input	3	21	Rx2n	Receiver Non-Inverted Data Output	3
3	Tx2p	Transmitter Non-Inverted Data Input	3	22	Rx2p	Receiver Inverted Data Output	3
4	GND	Ground [1]	1	23	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	3	24	Rx4n	Receiver Non-Inverted Data Output	3
6	Tx4p	Transmitter Non-Inverted Data Input	3	25	Rx4p	Receiver Inverted Data Output	3
7	GND	Ground [1]	1	26	GND	Ground [1]	1
8	ModSelL	Module Select	3	27	ModPrsL	Module Present	3
9	ResetL	Module Reset	3	28	IntL	Interrupt	3
10	Vcc Rx	+3.3V Power Supply Receiver [2]	2	29	Vcc Tx	+3.3V Power supply transmitter [2]	2
11	SCL	2-wire serial interface clock	3	30	Vcc1	+3.3V Power supply [2]	2
12	SDA	2-wire serial interface data	3	31	LPMode	Low Power Mode	3
13	GND	Ground [1]	1	32	GND	Ground [1]	1
14	Rx3p	Receiver Non-Inverted Data Output	3	33	Tx3p	Transmitter Inverted Data Input	3
15	Rx3n	Receiver Inverted Data Output	3	34	Tx3n	Transmitter Non-Inverted Data Input	3
16	GND	Ground	1	35	GND	Ground [1]	1
17	Rx1p	Receiver Non-Inverted Data Output	3	36	Tx1p	Transmitter Inverted Data Input	3
18	Rx1n	Receiver Inverted Data Output	3	37	Tx1n	Transmitter Non-Inverted Data Input	3
19	GND	Ground [1]	1	38	GND	Ground [1]	1

Notes:
1. GND is the symbol for signal supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

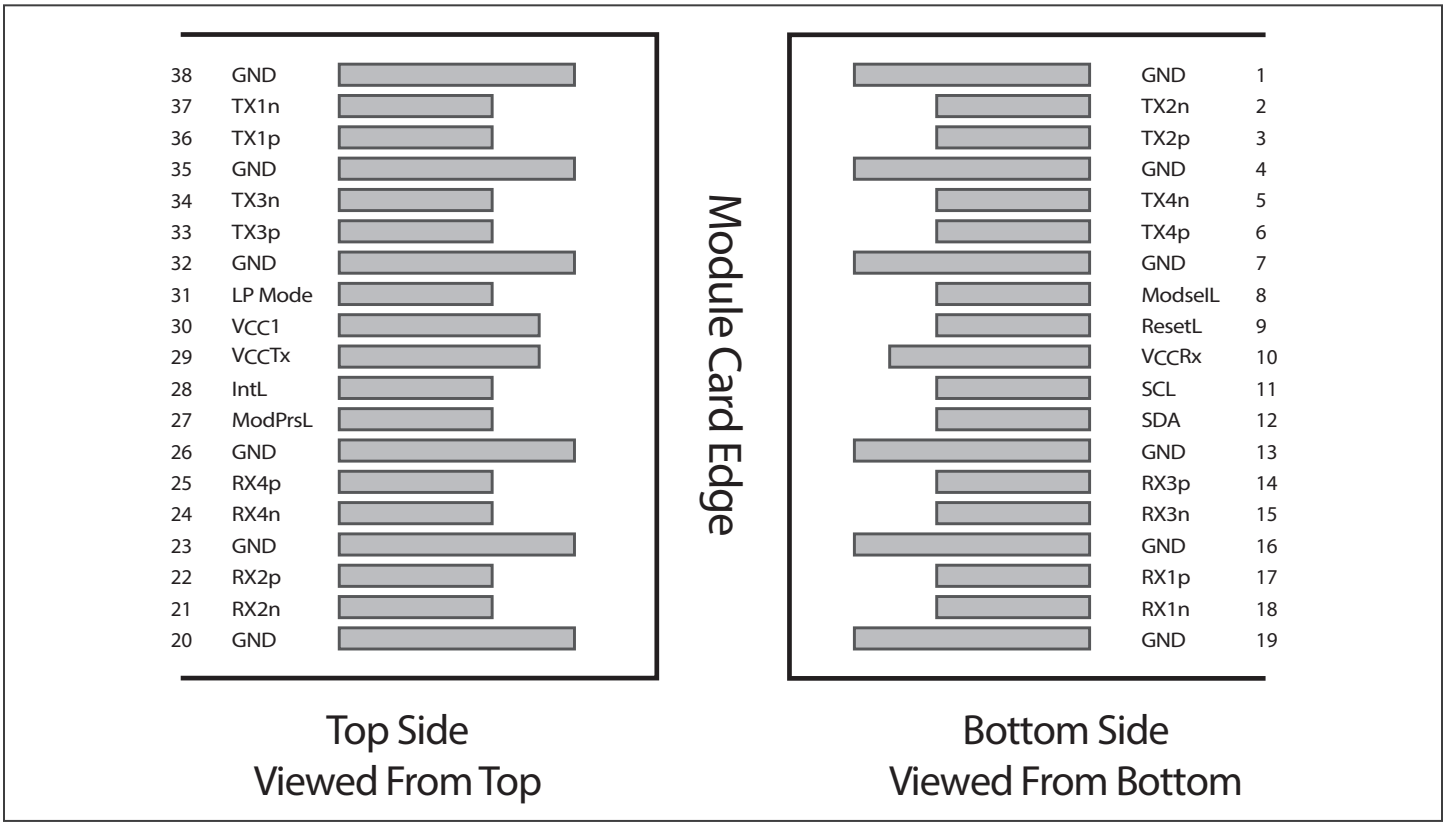


Figure 1 – QSFP+ MSA-compliant 38-pin connector

Application Notes

Electrical Interface: All signal interfaces are compliant with the QSFP+ MSA specification. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC.

ModSelL: The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ module is deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

ResetL: The ResetL signal is pulled to Vcc in the QSFP+ module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode: Low power mode. When held high by host, the module is held at low power mode. When held low by host, the module operates in the normal mode. For class 1 power level modules (1.5W), low power mode has no effect.

ModPrsL: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when module is inserted into the host connector, and deasserted "High" when the module is physically absent from the host connector.

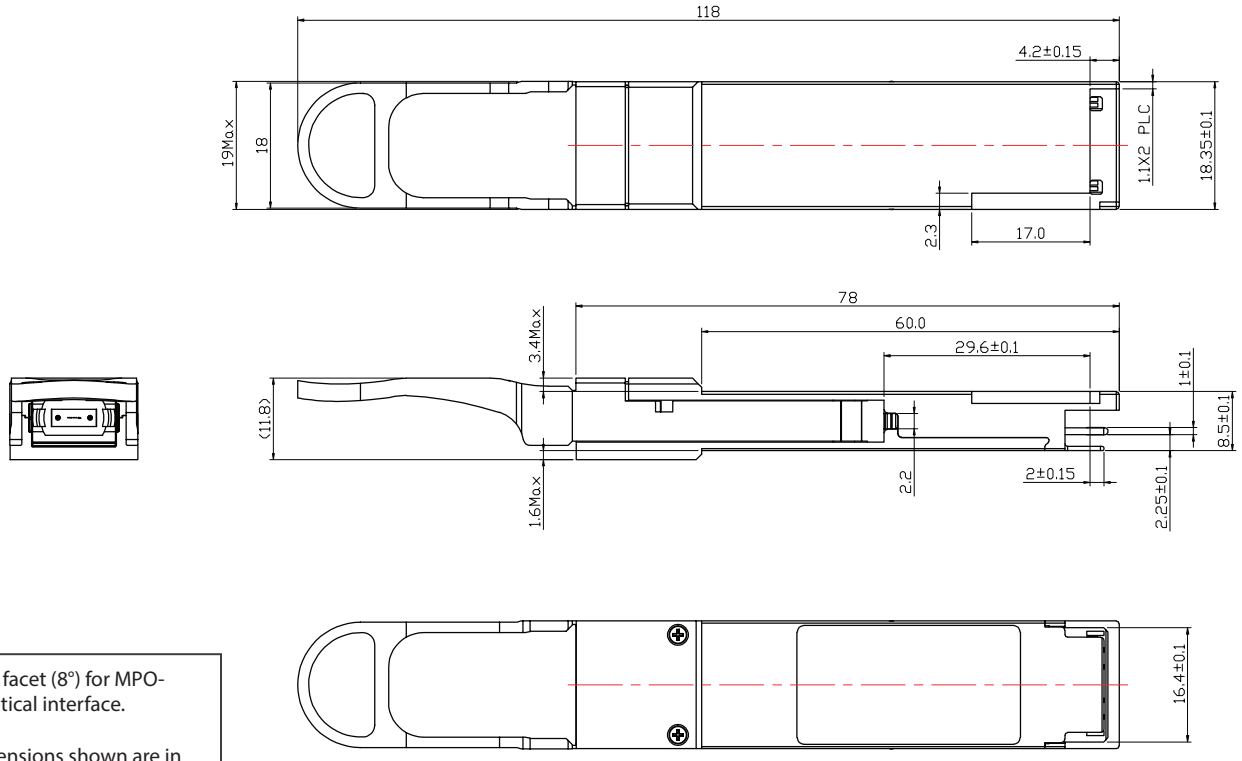
IntL: IntL is an output signal. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board. A corresponding soft status IntL signal is also available in the transceiver memory page 0 address 2 bit 1.

Receiver LOS: The receiver LOS status signal is on page 0 address 3 bits 0-3 for channels 1-4 respectively. Receiver LOS is based on input optical modulation amplitude (OMA). This status register is latched and it is cleared on read.

Transmitter Fault: The transmitter fault status signal is on page 0 address 4 bits 0-3 for channels 1-4 respectively. Conditions that lead to transmitter fault include laser fault, which occurs generally at transceiver end of life.

Transmitter Disable: The transmitter disable control is on page 0 address 86 bits 0-3 for channels 1-4 respectively. When in transmitter fault, toggling the transmitter disable bit signals the transmitter channel to exit the fault state and restores the channel function, unless fault condition persists.

Module Outline



Angled facet (8°) for MPO-MTP optical interface.

All dimensions shown are in millimetres. Tolerances are in accordance with QSFP+ MSA.

Notes:
* Trx length of 78mm is over MSA reference (72mm), exception for MSA compliance.

Ordering Information

Part Number	Operating Temperature		Nominal Wavelength	Distance	Latch Color	Notes
QSP1PF4LRC000E3G	- 5°C to + 70°C	Commercial	1310nm	10km	Blue	Multi rate
QSP1PF4LRC000E2G	- 5°C to + 70°C	Commercial	1310nm	10km	Blue	Single rate
QSP1PF4LLC000E2G	- 5°C to + 70°C	Commercial	1310nm	2km	Yellow	Single rate

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